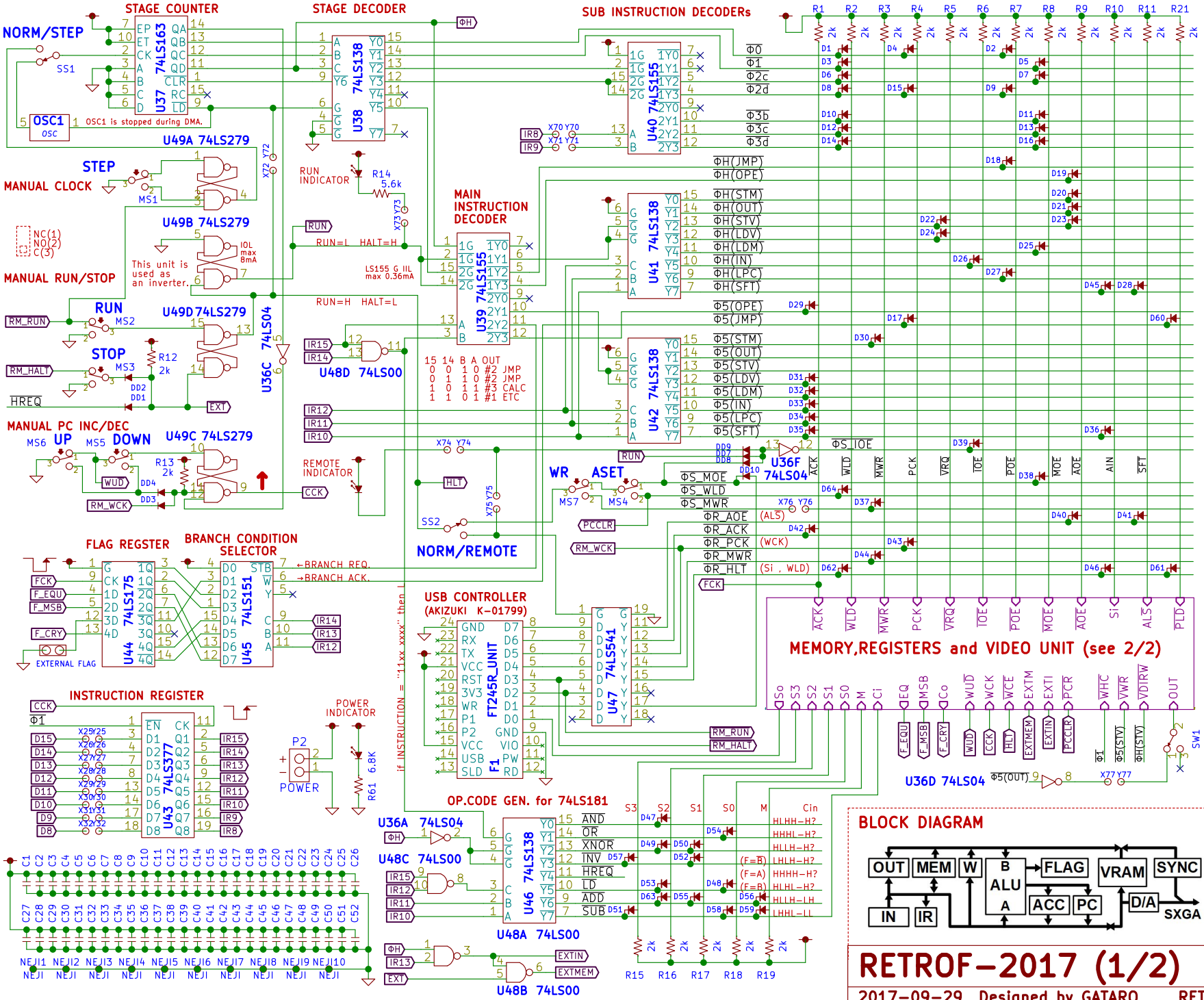
STAGE COUNTER
STAGE DECODER
SUB INSTRUCTION DECODERs
NORM/STEP
SS1
OSC1
OSC1 is stopped during DMA.
U37 74LS163
U38 74LS138
U40 74LS155
U49A 74LS279
STEP
MANUAL CLOCK
MS1
RUN INDICATOR
R14 5.6k
MAIN INSTRUCTION DECODER
U39 74LS155
U41 74LS138
U42 74LS138
NC(1)
NO(2)
C(3)
U49B 74LS279
This unit is used as an inverter.
MANUAL RUN/STOP
RUN
STOP
MS2
MS3
R12 2k
U49D 74LS279
U36C 74LS04
RM_RUN
RM_HALT
HREQ
EXT
RUN=L HALT=H
RUN=H HALT=L
LS155 G IIL max 0.36mA
15 14 B A OUT
0 0 1 0 #2 JMP
0 1 1 0 #2 JMP
1 0 1 1 #3 CALC
1 1 0 1 #1 ETC
U48D 74LS00
MANUAL PC INC/DEC
UP
DOWN
MS6
MS5
R13 2k
U49C 74LS279
WUD
RM_WCK
REMOTE INDICATOR
CCK
HLT
SS2
NORM/REMOTE
WR ASET
MS7
MS4
U36F 74LS04
PCCLR
RM_WCK
FCK
RUN
ΦS_MOE
ΦS_WLD
ΦS_MWR
ΦR_AOE (ALS)
ΦR_ACK
ΦR_PCK (WCK)
ΦR_MWR
ΦR_HLT (Si , WLD)
MEMORY,REGISTERS and VIDEO UNIT (see 2/2)
ACK WLD MWR PCK VRQ TOE POE MOE AOE Si ALS PLD
So S3 S2 S1 S0 M Ci EQU MSB Co WUD WCK WCE EXTM EXTI PCR WHC VWR VDTRW OUT
U36D 74LS04
ΦS(OUT)
FLAG REGSTER
BRANCH CONDITION SELECTOR
U44 74LS175
U45 74LS151
FCK
F_EQU
F_MSB
F_CRY
EXTERNAL FLAG
←BRANCH REQ.
→BRANCH ACK.
USB CONTROLLER
(AKIZUKI K-01799)
F1 FT245R_UNIT
U47 74LS541
if INSTRUCTION = "11xx xxxx" then L
INSTRUCTION REGISTER
U43 74LS377
POWER INDICATOR
P2
POWER
R61 6.8K
OP.CODE GEN. for 74LS181
U46 74LS138
U36A 74LS04
U48C 74LS00
U48A 74LS00
U48B 74LS00
AND
OR
XNOR
INV
HREQ
LD
ADD
SUB
HLHH-H?
HHHL-H?
HLLH-H?
LHLH-H?
HHHH-H?
HLHL-H?
HLLH-LH
LHHL-LL
EXTIN
EXTMEM
R15 R16 R17 R18 R19
NEJI1 NEJI2 NEJI3 NEJI4 NEJI5 NEJI6 NEJI7 NEJI8 NEJI9 NEJI10
INSTRACTION SET ARCH.
xxxx xxaa (common format)
aa=00 : 8bit immediate
aa=01 : register(0-255) direct
aa=10 : register(0-255) indirect
aa=11 : 16bit immediate
0ccc ddaa JMP
ccc=000 : ALWAY
ccc=001 : EXTERNAL
ccc=010 : Jump if FULL
ccc=011 : Jump if not FULL
ccc=100 : Jump if CARRY
ccc=101 : Jump if not CARRY
ccc=110 : Jump if MINUS
ccc=111 : Jump if not MINUS
dd=00 : wait request
dd=01 : absolute jump
dd=10 : relative jump (forward)
dd=11 : relative jump (backward)
11M0 00aa STM
11-0 01aa OUT
11-0 10aa STV
11-0 11aa LDV
11M1 00aa LDM
11P1 01-- IN
11-1 10-- LPC
11-1 11-- SFT
10-0 00aa HALT
10-0 01aa LD
10-0 10aa ADD
10-0 11aa SUB
10-1 00aa AND
10-1 01aa OR
10-1 10aa XNOR
10-1 11aa INV
M=1 EXTENDED MEMORY ACCESS
P=1 EXTENDED PORT ACCESS
SXGA VIDEO TIMMING CHART
H-SYNC (H9..H0) TIMING CHART
clock 27.000MHz
19+32+32+256+1=340clock
LOAD 10 1010 1101
10 1010 1110 FRONT-PORCH
10 1010 1111 19clock
10 1011 1111
10 1100 0000
10 1100 0001 HS
10 1100 0010 64clock (79.412KHz)
10 1101 1111
10 1110 0000
10 1110 0001 BACK-PORCH
10 1110 0010 64clock
10 1111 1111
11 0000 0000
11 0000 0001 PICTURE
11 0000 0010 AVAILABLE 256clock
11 1111 1111
00 0000 0000 LOAD REQUEST
V-SYNC (V9..V0) TIMING CHART
1clock=27.000MHz/340=79.411KHz
(256+2+2+4)*4=1056clock
CLEAR 00 0000 0000
00 0000 0001
00 0000 0010 PICTURE
00 0000 0011 AVAILABLE 256*4clock
00 1111 1111
0100 0000 00 FRONT-PORCH
0100 0000 01 2*4clock
0100 0000 10 VS 2*4clock
0100 0000 11 (75.199Hz)
0100 0001 00
0100 0001 01 BACK-PORCH
0100 0001 10 4*4clock
0100 0001 11
0100 0100 00 CLEAR
BLOCK DIAGRAM
OUT
MEM
W
B
ALU
A
FLAG
VRAM
SYNC
IN
IR
ACC
PC
D/A
SXGA
RETROF-2017 (1/2)
REV. (2.07B)
2017-09-29 Designed by GATARO
RETROF2017M.sch